Design Tips

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Welcome to Design Tips! In this issue, I will discuss the effect of mounting a capacitor on a printed circuit board on its performance. The capacitor's low equivalent series inductance (ESL) is only a small part of the overall story!

Please send me your most useful design tip for consideration in this section. Ideas should not be limited by anything other than your imagination! Please send these submissions to bruce.arch@ieee.org. I'll look forward to receiving many "Design Tips!" Please also let me know if you have any comments or suggestions for this section, or comments on the Design Tips articles.

Decoupling Capacitor Connection Inductance

By Bruce Archambeault, Ph.D.

It is very common for printed circuit board (PCB) designers, and EMC engineers who work with them, to use decoupling and filter capacitors with a low equivalent series inductance (ESL). Depending on the size of the surface mount capacitor, the values for ESL typically range from 0.2 nH to 0.5 nH. However, this is not the complete story on the inductance associated with decoupling capacitors! The connection inductance controls how effective the decoupling capacitor is for providing a charge to the power/ground-reference plane pair.

The connection inductance depends upon the distance between the vias and the distance from the top (or bottom) mounting location to the planes that are to be decoupled[1]. Figure 1 shows a side view of a typical decoupling capacitor mounting on a PCB.

It is obvious that if the vias are placed close together, and the planes to be decoupled are near the top of the PCB (when the capacitor is mounted on the top of the PCB), the connection inductance, represented by the loop, will be minimized. However, there are limits to how close the vias can be placed due to manufacturing issues. There are also limits to how close to the top surface the power/ground-reference planes can be located. So it is important to understand how the mounting will affect the performance of the capacitor and the connection inductance.

Connection inductance alone does not tell the complete story. The inductance associated with the spacing between the power/ground-plane pair, as well as any inductance associated with the distance between the IC and the decoupling capacitor, is not included in the connection inductance calculations.

Figures 2 and 3 show the 0603 and 0402 size capacitor mounting, respectively, for typical manufacturing limits. Table 1 shows some calculated[2] connection inductances (without ESL) for 0805, 0603, and 0402 size SMT capacitors for different depths to the power/ground-reference plane pairs [1–2].

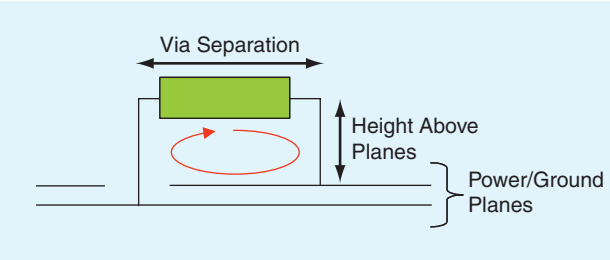

Fig 1. Typical Surface Mounted Decoupling Capacitor Loop Inductance

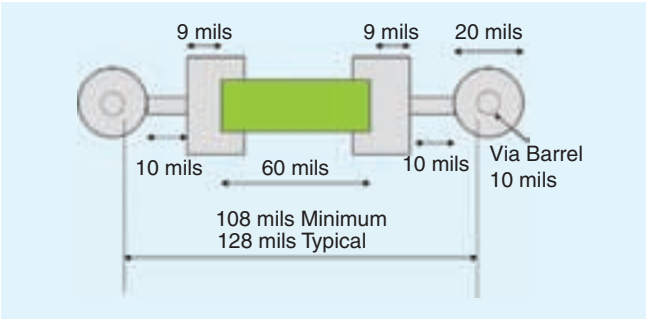

Fig 2. Typical Minimum 0603 Capacitor Mounting Dimensions

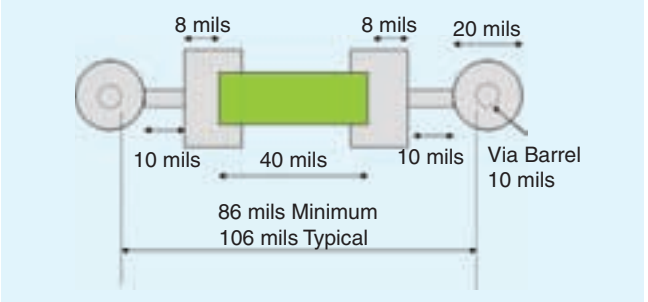

Fig 3. Typical Minimum 0402 Capacitor Mounting Dimensions

[1] Connection inductance is considered to be 'above the planes' only, and does not consider the separation between the power and ground planes, nor the distance from the capacitor to the observation point.

[2] See references for details on the formula used for this calculation.

TABLE 1. CONNECTION INDUCTANCE FOR TYPICAL CAPACITOR CONFIGURATIONS.

Distance into board to planes (mils)	0805 typical/minimum (148 mils between via barrels)	0603 typical/minimum (128 mils between via barrels)	0402 typical/minimum (106 mils between via barrels)
10	1.2 nH	1.1 nH	0.9 nH
20	1.8 nH	1.6 nH	1.3 nH
30	2.2 nH	1.9 nH	1.6 nH
40	2.5 nH	2.2 nH	1.9 nH
50	2.8 nH	2.5 nH	2.1 nH
60	3.1 nH	2.7 nH	2.3 nH
70	3.4 nH	3.0 nH	2.6 nH
80	3.6 nH	3.2 nH	2.8 nH
90	3.9 nH	3.5 nH	3.0 nH
100	4.2 nH	3.7 nH	3.2 nH

TABLE 2. CONNECTION INDUCTANCE FOR TYPICAL CAPACITOR CONFIGURATIONS WITH 50 MILS FROM CAPACITOR PAD TO VIA PAD.

Distance into board to planes (mils)	0805 (208 mils between via barrels)	0603 (188 mils between via barrels)	0402 (166 mils between via barrels)
10	1.7 nH	1.6 nH	1.4 nH
20	2.5 nH	2.3 nH	2.0 nH
30	3.0 nH	2.8 nH	2.5 nH
40	3.5 nH	3.2 nH	2.8 nH
50	3.9 nH	3.5 nH	3.1 nH
60	4.2 nH	3.9 nH	3.5 nH
70	4.5 nH	4.2 nH	3.7 nH
80	4.9 nH	4.5 nH	4.0 nH
90	5.2 nH	4.7 nH	4.3 nH
100	5.5 nH	5.0 nH	4.6 nH

These values are calculated with the example of 7–8 mils from capacitor-to-mounting-pad-edge, 20 mils from capacitor-mounting-pad-edge-to-via-pad, via pad diameter of 20 mils, via barrel size of 10 mils, and trace width equal to 20 mils. The absolute minimum distance from the via pad to capacitor mounting pad edge is reported to be 10 mils, but typically 20 mils is used to be 'safe'.

The distance between the via pad and the capacitor mounting pad was kept to a small value in the above calculations. If this distance is increased slightly to 50 mils, the connection inductance increases to the values shown in Table 2.

Summary

The connection inductance plays a much greater role in the performance of decoupling capacitors than the typical ESL of these components. Typical connection inductance values of one to three nanoHenries are typical with common surface mount capacitor sizes and typical manufacturing technologies. Using the tables, engineers can decide if a decoupling capacitor is better placed on the top or bottom surface of the PCB in order to best provide charge to the power/ground-reference plane pairs.

References

[1] J. L. Knighten, B. Archambeault, J. Fan, S. Connor, and J. L. Drewniak. PDN design strategies: II. Ceramic SMT decoupling capacitors – Does location matter?, *IEEE EMC Soc. Newslett.* (Winter 2006). Issue 208, pp. 56–67. Available: www.emcs.org

[2] J. Fan, C. Wei, J. L. Drewniak, T. Van Doren, and J. L. Knighten, "Estimating the noise mitigating effect of local decoupling in printed circuit boards," *IEEE Trans. Adv. Packag.*, vol. 25, no. 2, pp. 154–165, May 2002.

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